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*4/2-02*  
**PATENT**

jc879 U.S. PTO  
10/000479  
10/24/01

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**In re Application of:**

Jigish D. Trivedi et al.

**Serial No.:** Not Yet Assigned

**Filed:** October 24, 2001

**For:** LOCAL INTERCONNECT  
STRUCTURE FOR INTEGRATED CIRCUIT  
DEVICES, SOURCE STRUCTURE FOR THE  
SAME, AND METHOD FOR FABRICATING  
THE SAME

**Examiner:** Unknown

**Group Art Unit:** Unknown

**Attorney Docket No.:** 3439.4US (97-936.3)

**NOTICE OF EXPRESS MAILING**

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**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
Washington, D.C. 20231

Sir:

The present application is a divisional of application Serial No. 09/055,056, filed April 3, 1998, pending.

Pursuant to M.P.E.P. 2001.06(b), the Examiner is respectfully requested to consider the information of record in the prior application, and to confirm in the first Office Action on the merits that such art has in fact been reviewed. A PTO-1449 form listing all of the information of record in the prior application is enclosed herewith.

This Information Disclosure Statement is filed within three (3) months of the filing date of the above-identified application, and no certification pursuant to 37 C.F.R. § 1.97(c) or a fee pursuant to 37 C.F.R. 1.17(p) is required.

Respectfully submitted,



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Date: October 24, 2001

KAH/ps:dlm

Enclosure: Form PTO-1449

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